Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.080”**

**.080”**

**ANODE**

**.065” X .065”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .004” X .004”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .080” X .080” DATE: 9/21/21**

**MFG: ON SEMI THICKNESS .015” P/N: MURC820**

**DG 10.1.2**

#### Rev B, 7/1